

# 74LVC169

## Presettable synchronous 4-bit up/down binary counter

Rev. 04 — 14 October 2004

Product data sheet

### 1. General description

The 74LVC169 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

The 74LVC169 is a synchronous presettable 4-bit binary counter which features an internal look-ahead carry circuitry for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the output (pins Q0 to Q3) change coincident with each other when so instructed by the count-enable (pins  $\overline{CEP}$  and  $\overline{CET}$ ) inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock (pin CP) input triggers the four flip-flops on the LOW-to-HIGH transition of the clock. The counter is fully programmable; that is, the outputs may be preset to any number between 0 and its maximum count. Presetting is synchronous with the clock and takes place regardless of the levels of the count enable inputs. A LOW level on the parallel enable (pin  $\overline{PE}$ ) input disables the counter and causes the data at the Dn input to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The direction of the counting is controlled by the up/down (pin  $U/\overline{D}$ ) input. When pin  $U/\overline{D}$  is HIGH, the counter counts up, when LOW, it counts down. The look-ahead carry circuitry is provided for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable (pins  $\overline{CEP}$  and  $\overline{CET}$ ) inputs and a terminal count (pin  $\overline{TC}$ ) output. Both count-enable (pins  $\overline{CEP}$  and  $\overline{CET}$ ) inputs must be LOW to count. Input pin  $\overline{CET}$  is fed forward to enable the terminal count (pin  $\overline{TC}$ ) output. Pin  $\overline{TC}$  thus enabled will produce a LOW-level output pulse with a duration approximately equal to a HIGH level portion of pin Q0 output. The LOW level pin  $\overline{TC}$  pulse is used to enable successive cascaded stages. The 74LVC169 use edge triggered J-K type flip-flops and have no constraints on changing the control of data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the next LOW-to-HIGH transition of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the mode select table. When pin  $\overline{PE}$  is LOW, the data on the input pins D0 to D3 enter the flip-flops on the next LOW-to-HIGH transition of the clock. In order for counting to occur, both pins  $\overline{CEP}$  and  $\overline{CET}$  must be LOW and pin  $\overline{PE}$  must be HIGH. The pin  $U/\overline{D}$  input determines the direction of the counting. The terminal count output pin  $\overline{TC}$  output is normally HIGH and goes LOW, provided that pin  $\overline{CET}$  is LOW, when a counter reaches 15 in the count up mode. The pin  $\overline{TC}$  output state is not a function of the count-enable parallel (pin  $\overline{CEP}$ ) input level. Since pin  $\overline{TC}$  signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on pin  $\overline{TC}$ . For this reason the use of pin  $\overline{TC}$  as a clock signal is not recommended; see the following logic equations:

$$\text{count enable} = \overline{CEP} \times \overline{CET} \times \overline{PE}$$

$$\text{count up: TC} = Q_3 \times Q_2 \times Q_1 \times Q_0 \times \overline{CET} \times (U/\overline{D})$$

$$\text{count down: TC} = \overline{Q_3} \times \overline{Q_2} \times \overline{Q_1} \times \overline{Q_0} \times \overline{CET} \times (\overline{U}/D).$$

**PHILIPS**

## 2. Features

- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- Complies with JEDEC standard JESD8-B/JESD36
- Up/down counting
- Two count enable inputs for n-bit cascading
- Built-in look-ahead carry capability
- Presetable for programmable operation
- ESD protection:
  - ◆ HBM EIA/JESD22-A114-B exceeds 2000 V
  - ◆ MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

## 3. Quick reference data

**Table 1: Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$	propagation delay	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$				
$t_{PLH}$	CP to $Q_n$		-	4.0	-	ns
	CP to $\overline{TC}$		-	4.8	-	ns
	$\overline{CET}$ to $\overline{TC}$		-	4.1	-	ns
	$U/\overline{D}$ to $\overline{TC}$		-	3.7	-	ns
$f_{max}$	maximum clock frequency		-	200	-	MHz
$C_I$	input capacitance		-	5.0	-	pF
$C_{PD}$	power dissipation capacitance per gate		[1] [2]	20	-	pF

[1]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacity in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

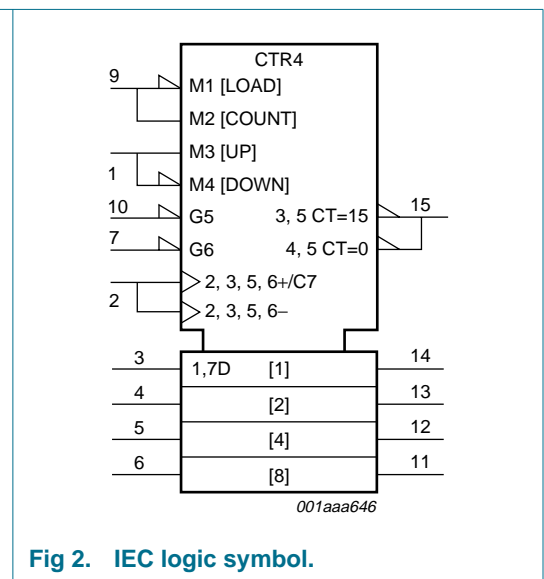
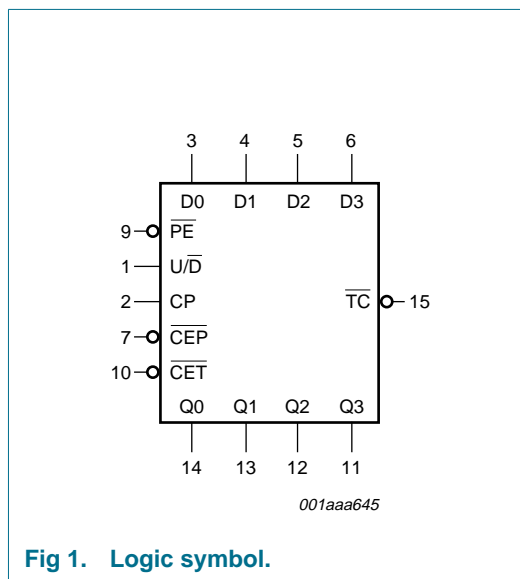
[2] The condition is  $V_I = GND$  to  $V_{CC}$ .

### 4. Ordering information

Table 2: Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74LVC169D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC169DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC169PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC169BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

### 5. Functional diagram



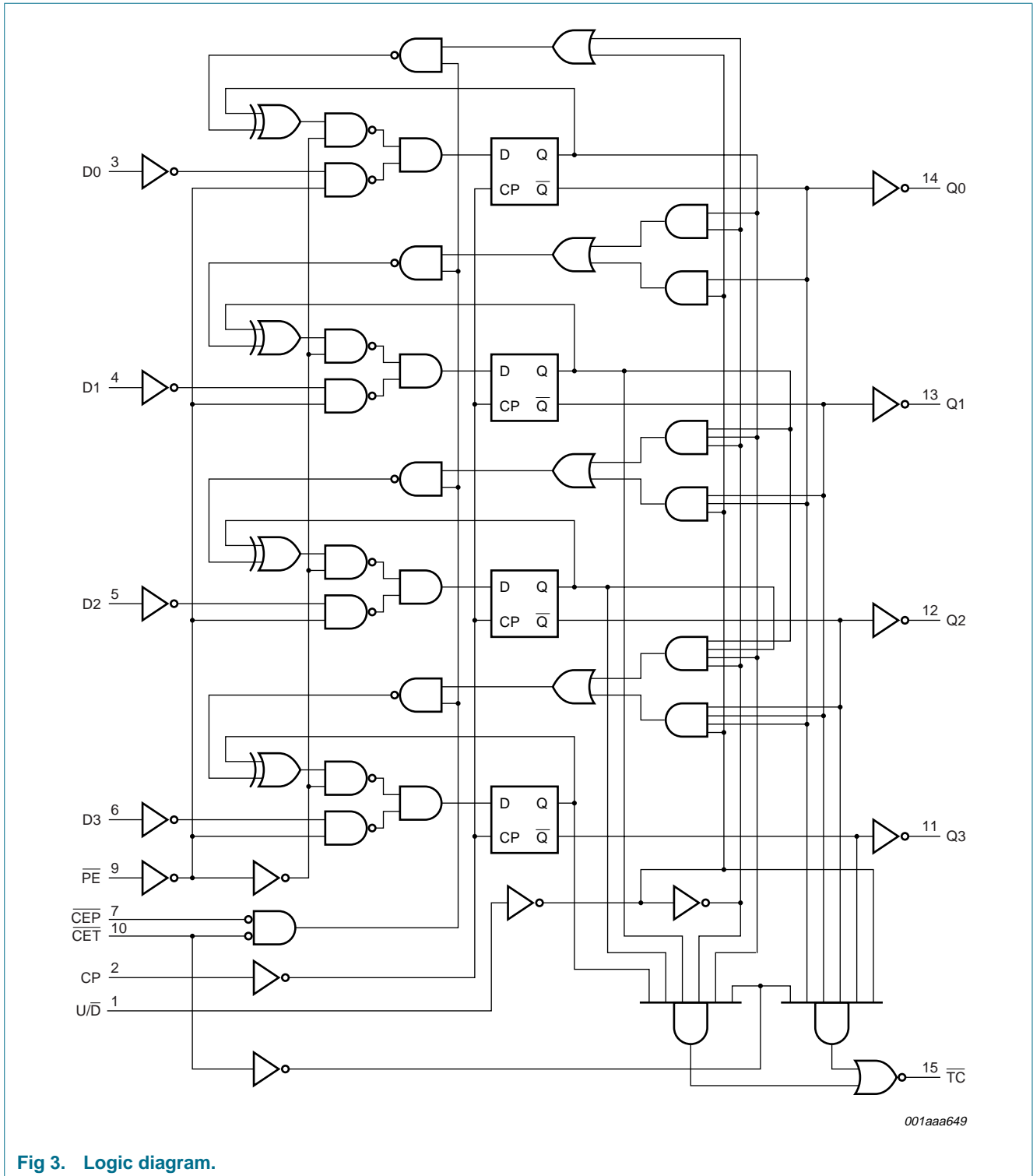


Fig 3. Logic diagram.

## 6. Pinning information

### 6.1 Pinning

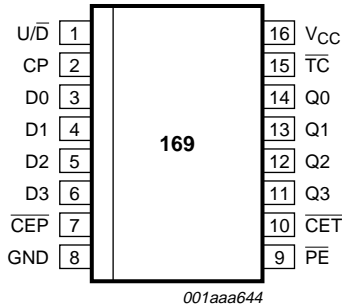


Fig 4. Pin configuration SO16 and (T)SSOP16 package.

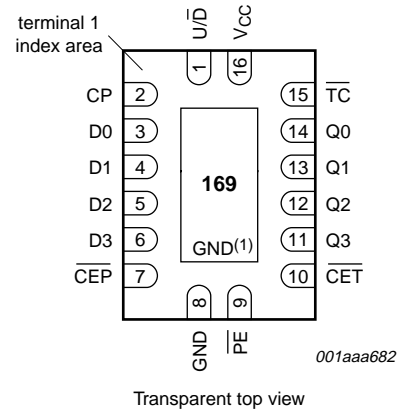


Fig 5. Pin configuration DHVQFN16 package.  
 (1) The die substrate is attached to this pad using conductive die material. It can not be used as a supply pin or input.

### 6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
U/D	1	up/down control input
CP	2	clock input (LOW-to-HIGH, edge-triggered)
D0	3	data input
D1	4	data input
D2	5	data input
D3	6	data input
CEP	7	count enable input (active LOW)
GND	8	ground (0V)
PE	9	parallel enable input (active LOW)
CET	10	count enable carry input (active LOW)
Q3	11	flip-flop output
Q2	12	flip-flop output
Q1	13	flip-flop output
Q0	14	flip-flop output
TC	15	terminal count output (active LOW)
V <sub>CC</sub>	16	supply voltage

## 7. Functional description

### 7.1 Function table

Table 4: Function table [1]

Operating modes	Input						Output	
	CP	U/D	CEP	CET	PE	Dn	Qn	TC
Parallel load (Dn → Qn)	↑	X	X	X	l	l	L	*
	↑	X	X	X	l	h	H	*
Count up (increment)	↑	h	l	l	h	X	count up	*
Count down (decrement)	↑	l	l	l	h	X	count down	*
Hold (do nothing)	↑	X	h	X	h	X	qn	*
	↑	X	X	X	h	X	qn	H

- [1] H = HIGH voltage level steady state.  
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.  
 L = LOW voltage level steady state.  
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.  
 qn = Lower case letters indicate state of referenced output prior to the LOW-to-HIGH clock transition.  
 X = Don't care.  
 ↑ = LOW-to-HIGH clock transition.  
 \* = The TC is LOW when CET is LOW and the counter is at terminal count.  
 Terminal count up is (HHHH) and terminal count down is (LLLL).

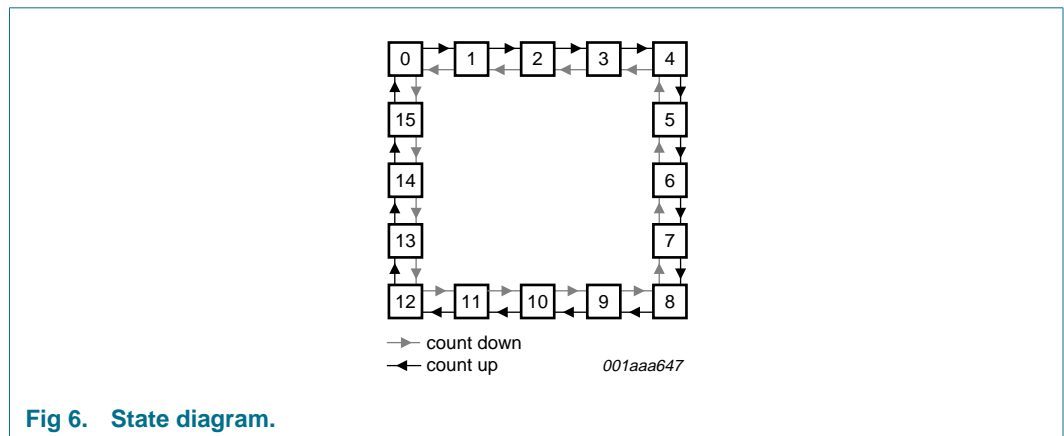
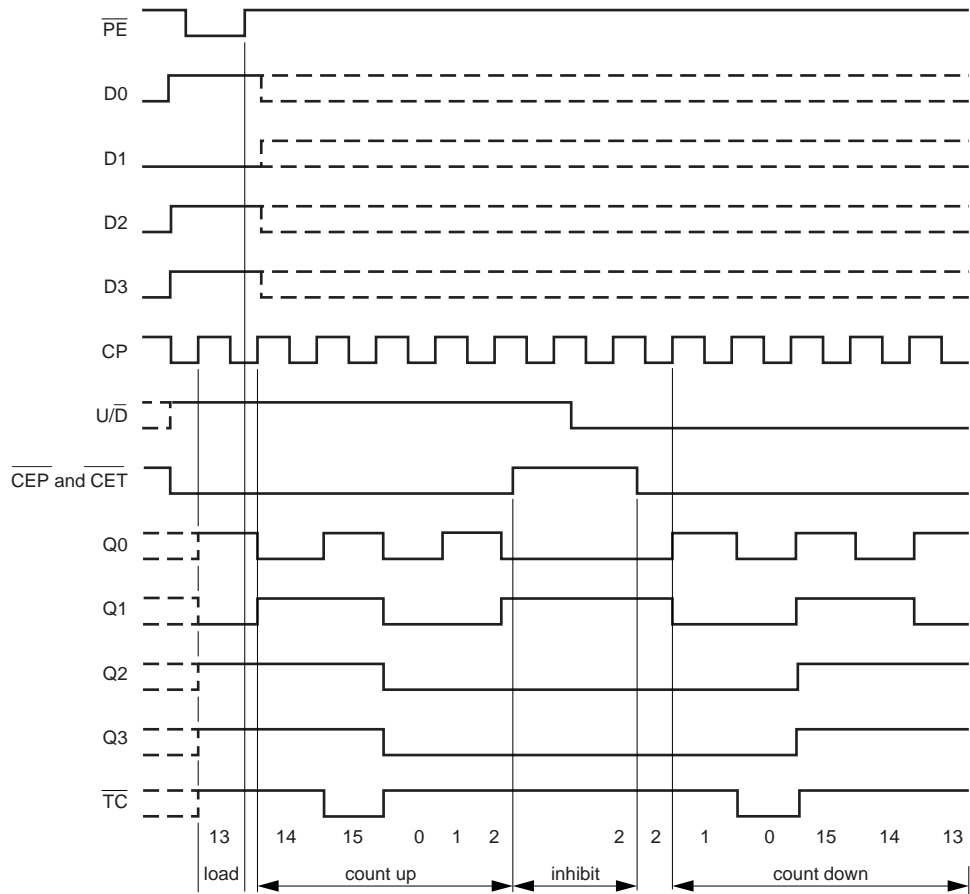


Fig 6. State diagram.



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Illustrated is the following sequence:

- Load (preset) to thirteen.
- count up to fourteen, fifteen (maximum), zero, one and two.
- Inhibit.
- Countdown to one, zero (minimum), fifteen, fourteen and thirteen.

**Fig 7. Typical timing sequence.**

## 8. Limiting values

**Table 5: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$ V	-	-50	mA
$V_I$	input voltage		[1] -0.5	+5.5	V
$I_{OK}$	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage		[1] -0.5	$V_{CC} + 0.5$	V
$I_O$	output source or sink current		-	$\pm 50$	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current	$V_O = 0$ V to $V_{CC}$	-	$\pm 100$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C,  $P_{tot}$  derates linearly with 8 mW/K.

For (T)SSOP16 packages: above 60 °C,  $P_{tot}$  derates linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C,  $P_{tot}$  derates linearly with 4.5 mW/K.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage		0	$V_{CC}$	V
$T_{amb}$	operating temperature	free-air	-40	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.2$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	0	10	ns/V

## 10. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to +85 °C [1]						
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2$ V	$V_{CC}$	-	-	V
		$V_{CC} = 2.7$ V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2$ V	-	-	GND	V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	0.8	V



**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	-	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.6	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	-	GND	0.2	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	μA
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	μA
C <sub>I</sub>	input capacitance		-	5.0	-	pF
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	GND	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	V <sub>CC</sub> - 0.3	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.65	-	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.75	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.3	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.6	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND	-	-	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	-	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	-	5000	μA

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**

$GND = 0\text{ V}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 500\ \Omega$ ; see [Figure 13](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b><math>T_{\text{amb}} = -40\text{ °C to }+85\text{ °C}</math> [1]</b>							
$t_{\text{PHL}}$ , $t_{\text{PLH}}$	propagation delay CP to Qn	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 1.2\text{ V}$	-	17	-	ns	
		$V_{\text{CC}} = 2.7\text{ V}$	1.5	-	7.2	ns	
	propagation delay CP to $\overline{\text{TC}}$	$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 1.5	4.0	8.0	ns	
		see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 1.2\text{ V}$	-	21	-	ns	
		$V_{\text{CC}} = 2.7\text{ V}$	1.5	-	8.8	ns	
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 1.5	4.8	6.7	ns	
		propagation delay $\overline{\text{CET}}$ to $\overline{\text{TC}}$	see <a href="#">Figure 9</a>				
$V_{\text{CC}} = 1.2\text{ V}$	-		19	-	ns		
$V_{\text{CC}} = 2.7\text{ V}$	1.5		-	7.2	ns		
$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 1.5		4.1	7.2	ns		
propagation delay U/ $\overline{\text{D}}$ to $\overline{\text{TC}}$	see <a href="#">Figure 10</a>						
	$V_{\text{CC}} = 1.2\text{ V}$		-	21	-	ns	
	$V_{\text{CC}} = 2.7\text{ V}$	1.5	-	8.2	ns		
	$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 1.5	3.7	7.0	ns		
	$t_{\text{W}}$	clock pulse width HIGH or LOW	see <a href="#">Figure 8</a>				
			$V_{\text{CC}} = 2.7\text{ V}$	5.0	-	-	ns
$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$			[2] 4.0	1.2	-	ns	
$t_{\text{su}}$	set-up time Dn to CP	see <a href="#">Figure 11</a>					
		$V_{\text{CC}} = 2.7\text{ V}$	3.0	-	-	ns	
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 2.5	1.0	-	ns	
	set-up time $\overline{\text{PE}}$ to CP	see <a href="#">Figure 11</a>					
		$V_{\text{CC}} = 2.7\text{ V}$	3.5	-	-	ns	
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 3.0	1.2	-	ns	
	set-up time U/ $\overline{\text{D}}$ to CP	see <a href="#">Figure 12</a>					
		$V_{\text{CC}} = 2.7\text{ V}$	6.5	-	-	ns	
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 5.5	2.8	-	ns	
	set-up time $\overline{\text{CEP}}$ , $\overline{\text{CET}}$ to CP	see <a href="#">Figure 12</a>					
		$V_{\text{CC}} = 2.7\text{ V}$	5.5	-	-	ns	
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 4.5	2.1	-	ns	
$t_{\text{h}}$	hold time Dn, $\overline{\text{PE}}$ , $\overline{\text{CEP}}$ , $\overline{\text{CET}}$ , U/ $\overline{\text{D}}$ to CP	see <a href="#">Figure 11</a> and <a href="#">12</a>					
		$V_{\text{CC}} = 2.7\text{ V}$	0.0	-	-	ns	
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 0.5	0.0	-	ns	
$f_{\text{max}}$	maximum clock pulse frequency	see <a href="#">Figure 8</a>					
		$V_{\text{CC}} = 2.7\text{ V}$	150	-	-	MHz	
		$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$	[2] 150	200	-	MHz	

**Table 8: Dynamic characteristics ...continued**  
 $GND = 0\text{ V}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 500\ \Omega$ ; see [Figure 13](#).

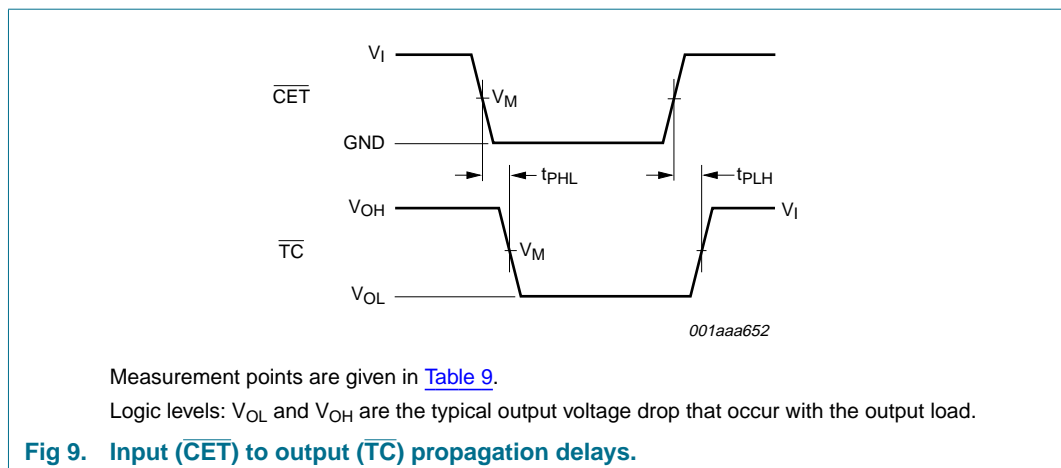
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sk(0)}$	skew	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[3] -	-	1.0	ns
$C_{PD}$	power dissipation capacitance per gate		[4] [5] -	20	-	pF
<b><math>T_{amb} = -40\text{ °C to }+125\text{ °C}</math></b>						
$t_{PHL}, t_{PLH}$	propagation delay CP to Qn	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.7\text{ V}$	1.5	-	9.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	10.0	ns
	propagation delay CP to $\overline{TC}$	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.7\text{ V}$	1.5	-	11.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	8.5	ns
	propagation delay $\overline{CET}$ to $\overline{TC}$	see <a href="#">Figure 9</a>				
		$V_{CC} = 2.7\text{ V}$	1.5	-	9.0	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	9.0	ns
	propagation delay U/ $\overline{D}$ to $\overline{TC}$	see <a href="#">Figure 10</a>				
		$V_{CC} = 2.7\text{ V}$	1.5	-	10.5	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.5	-	9.0	ns
$t_W$	clock pulse width HIGH or LOW	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.7\text{ V}$	5.0	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4.0	-	-	ns
$t_{su}$	set-up time Dn to CP	see <a href="#">Figure 11</a>				
		$V_{CC} = 2.7\text{ V}$	3.0	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	2.5	-	-	ns
	set-up time $\overline{PE}$ to CP	see <a href="#">Figure 11</a>				
		$V_{CC} = 2.7\text{ V}$	3.5	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	3.0	-	-	ns
	set-up time U/ $\overline{D}$ to CP	see <a href="#">Figure 12</a>				
		$V_{CC} = 2.7\text{ V}$	6.5	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	5.5	-	-	ns
	set-up time $\overline{CEP}, \overline{CET}$ to CP	see <a href="#">Figure 12</a>				
		$V_{CC} = 2.7\text{ V}$	5.5	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	4.5	-	-	ns
$t_h$	hold time Dn, $\overline{PE}$ , $\overline{CEP}$ , $\overline{CET}$ , U/ $\overline{D}$ to CP	see <a href="#">Figure 11</a> and <a href="#">12</a>				
		$V_{CC} = 2.7\text{ V}$	0.0	-	-	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	0.5	-	-	ns
$f_{max}$	maximum clock pulse frequency	see <a href="#">Figure 8</a>				
		$V_{CC} = 2.7\text{ V}$	150	-	-	MHz
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	150	-	-	MHz
$t_{sk(0)}$	skew	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	[3] -	-	1.5	ns

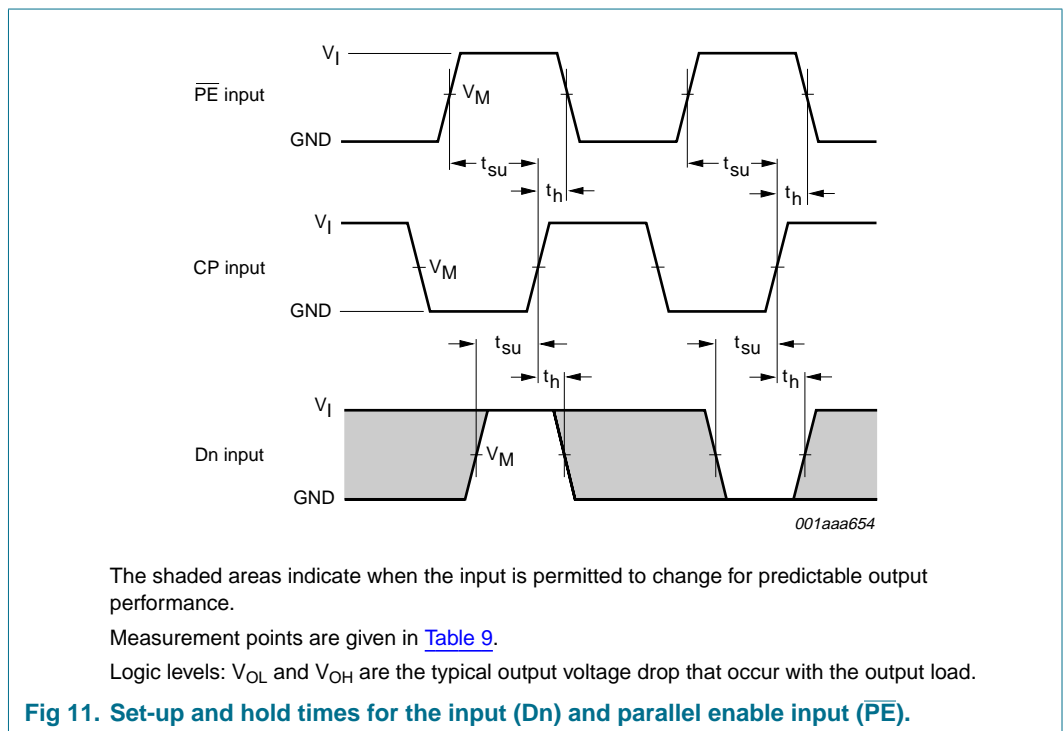
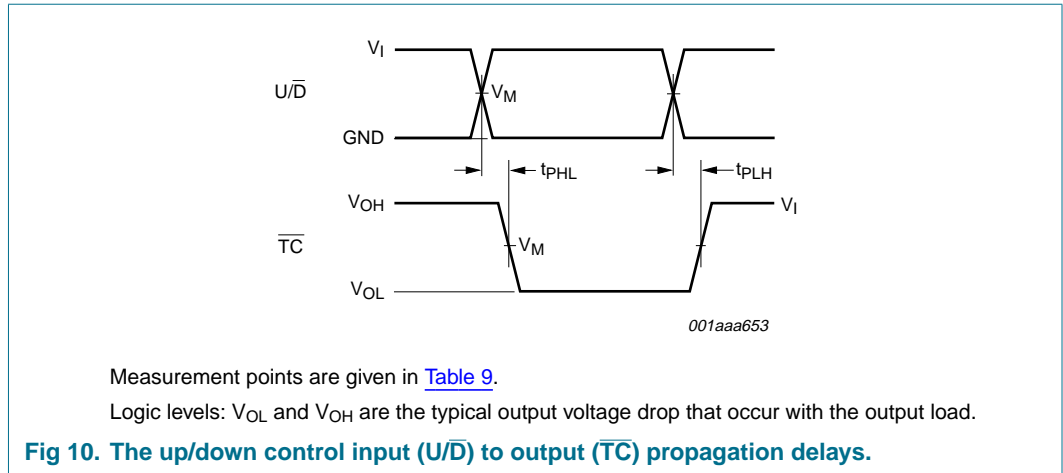
[1] All typical values are measured at  $T_{amb} = 25\text{ °C}$ .

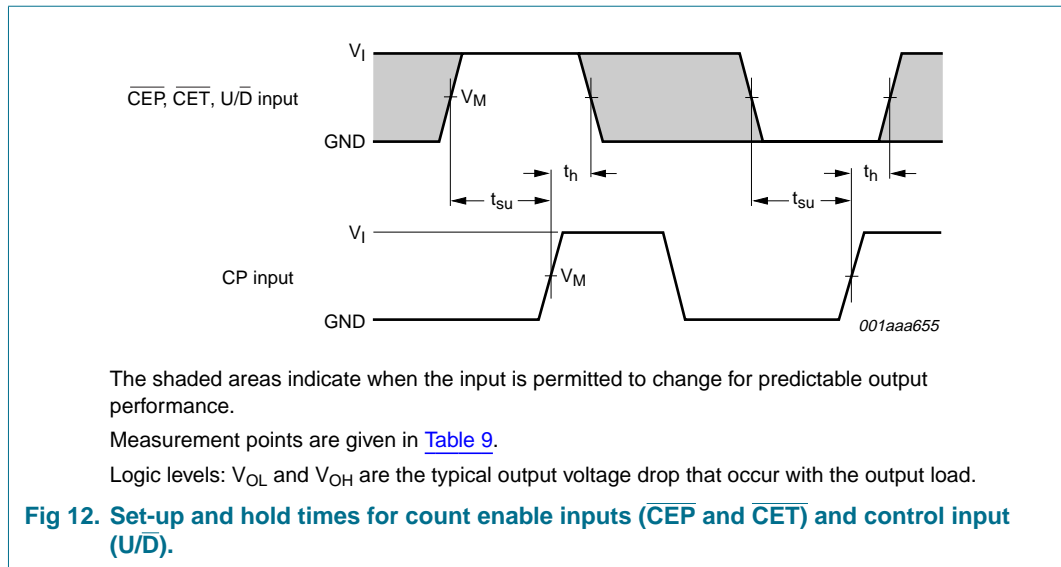
[2] Typical values are measured at  $V_{CC} = 3.3\text{ V}$ .

- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  
 $f_o$  = output frequency in MHz;  
 $C_L$  = output load capacity in pF;  
 $V_{CC}$  = supply voltage in Volts;  
 $N$  = total load switching outputs;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- [5] The condition is  $V_I = GND$  to  $V_{CC}$ .

## 12. Waveforms

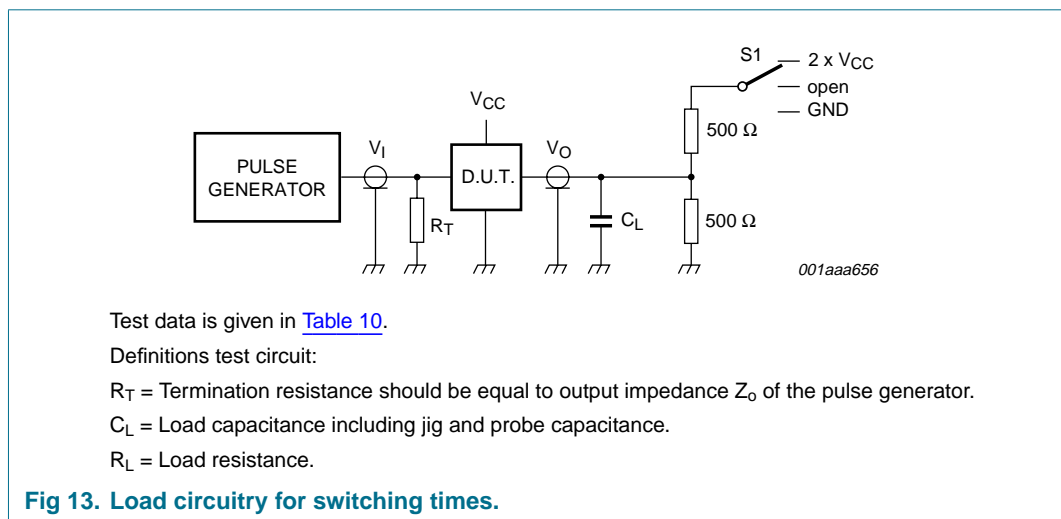






**Table 9: Measurement points**

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V



**Table 10: Measurement points**

Supply voltage	Input	Load		Position S1		
$V_{CC}$	$V_I$	$C_L$	$R_L$	$t_{PLH}$ , $t_{PHL}$	$t_{PZH}$ , $t_{PHZ}$	$t_{PZL}$ , $t_{PLZ}$
1.2 V	$V_{CC}$	50 pF	500 $\Omega$ [1]	open	GND	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$
3.0 V to 3.6 V	2.7 V	50 pF	500 $\Omega$	open	GND	$2 \times V_{CC}$

[1] The circuit performs better when  $R_L = 1000 \Omega$ .

13. Application information

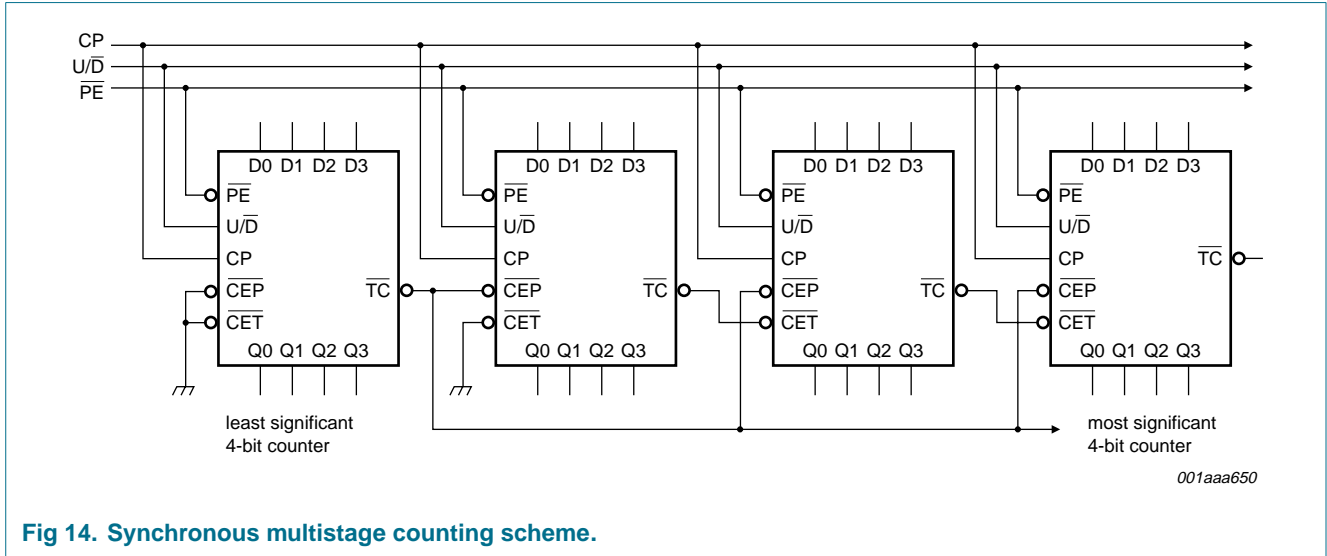


Fig 14. Synchronous multistage counting scheme.

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

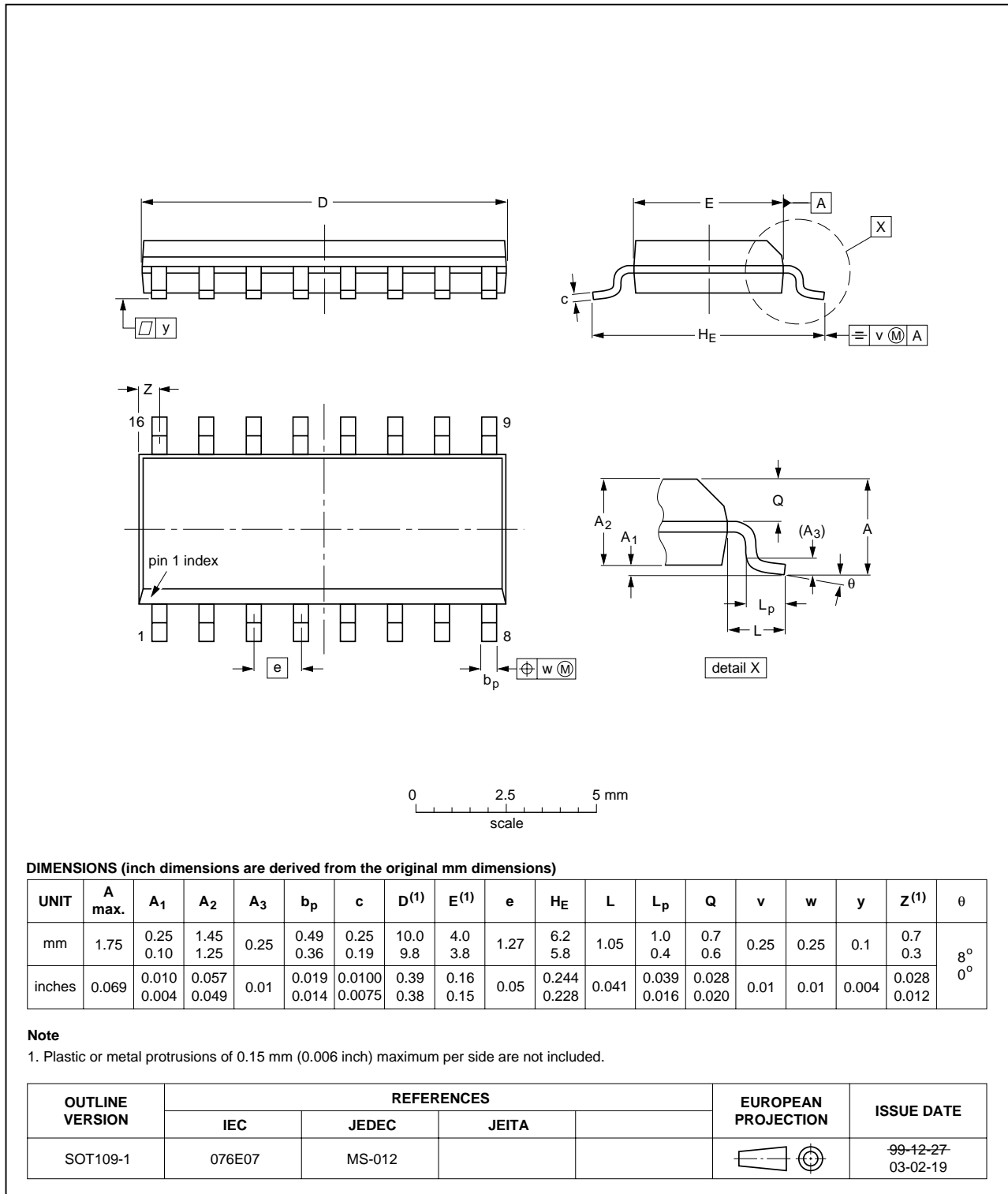


Fig 15. Package outline SOT109-1 (SO16).



SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

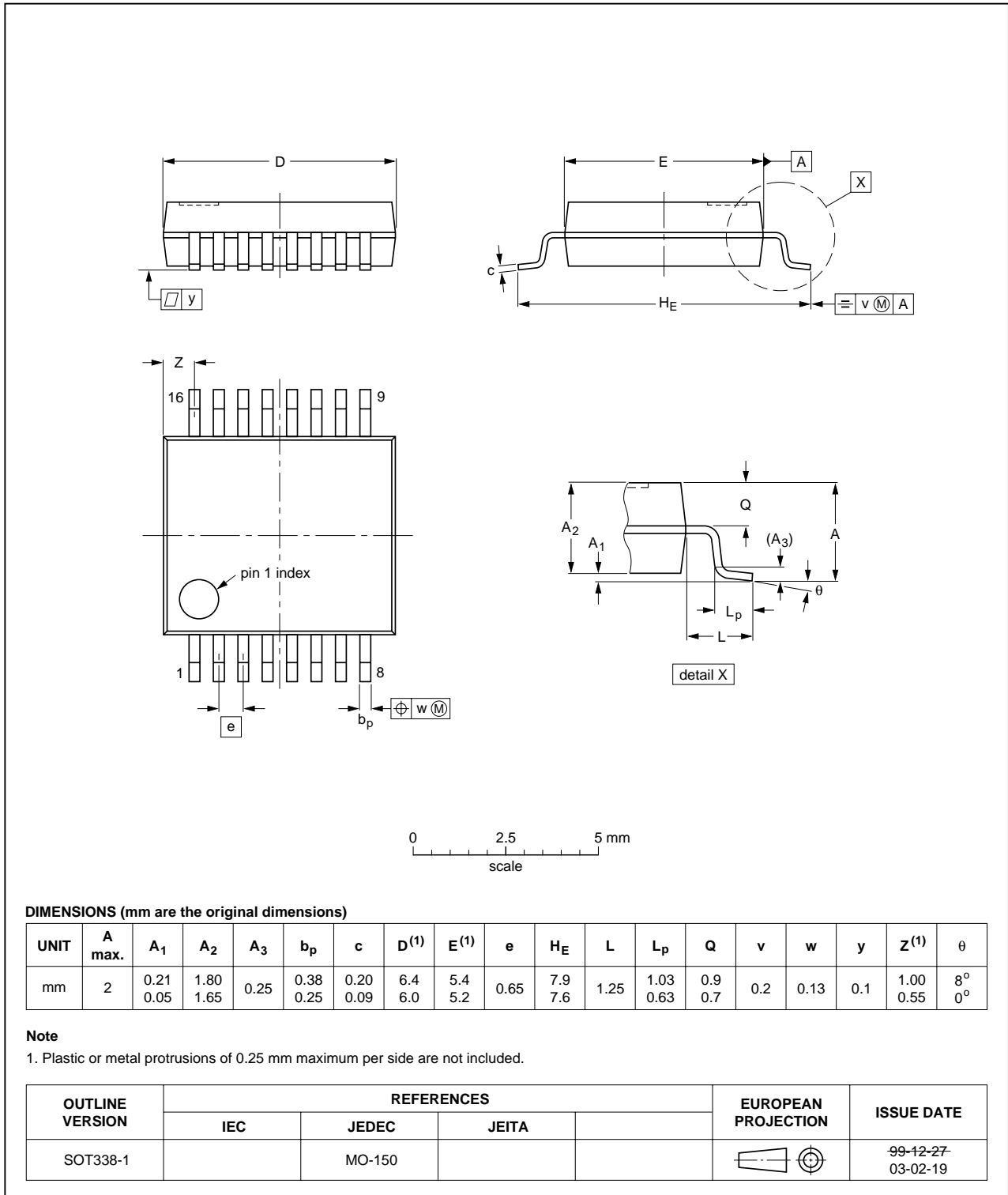


Fig 16. Package outline SOT338-1 (SSOP16).

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

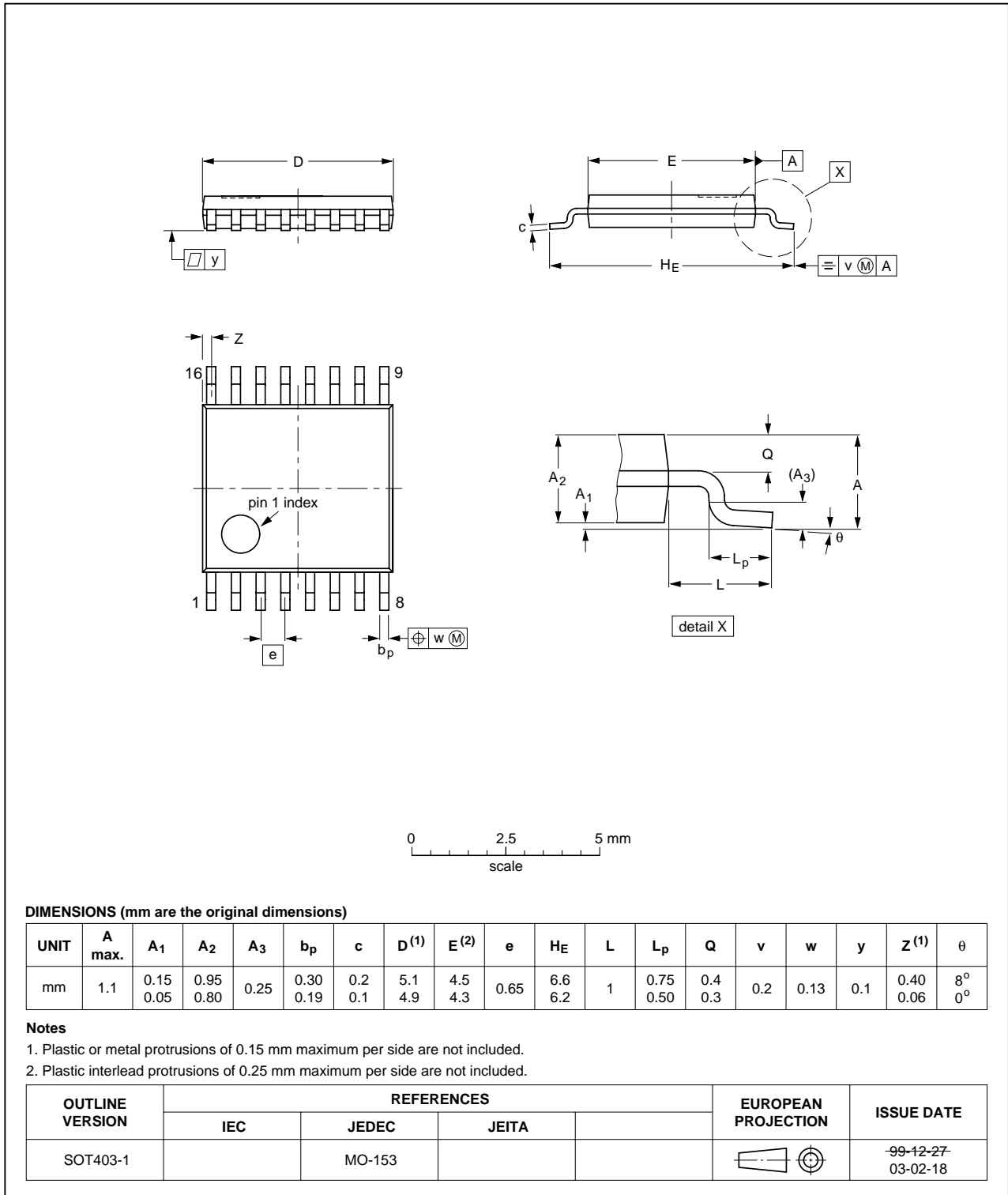


Fig 17. Package outline SOT403-1 (TSSOP16).

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

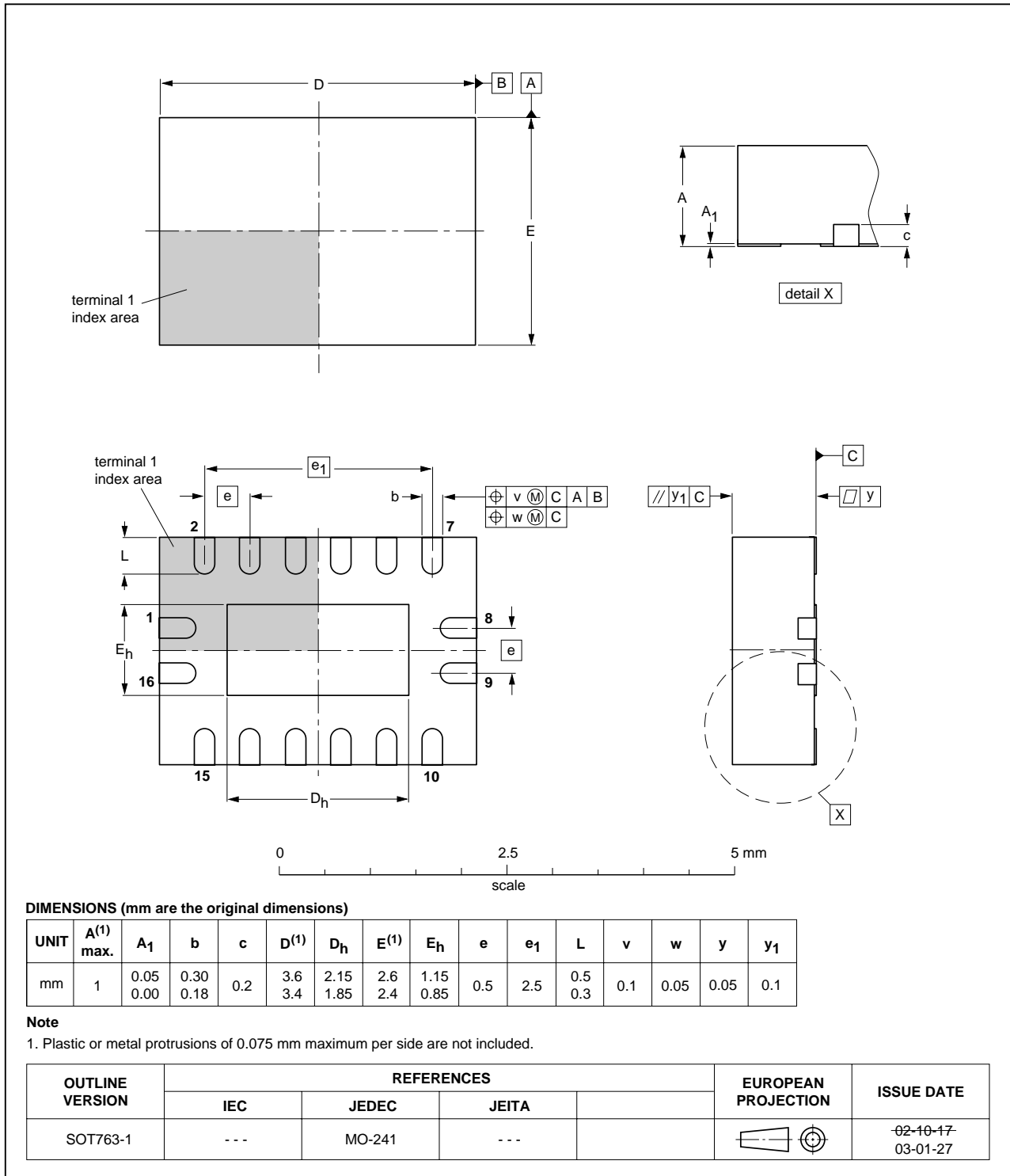


Fig 18. Package outline SOT763-1 (DHVQFN16).

## 15. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC169_4	14102004	Product data sheet	-	9397 750 13818	74LVC169_3
Modifications:	<ul style="list-style-type: none"><li>• Added DHVQFN16 package</li><li>• <a href="#">Section 1</a>: corrected logic equations</li><li>• <a href="#">Figure 14</a>: corrected connections between 1st and 2nd counter.</li></ul>				
74LVC169_3	20040512	Product data sheet	-	9397 750 13026	74LVC169_2
74LVC169_2	19980520	Product specification		9397 750 04498	74LVC169_1

## 16. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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